Also attached hereto is an Excess Claims Fee Payment Letter and fee.

Claims 1-27 are all of the claims pending in the present Application. New claims 21-27 have been added. Claims 1-20 stand rejected under 35 USC §112, second paragraph, as indefinite. Claims 1-20 stand rejected under 35 USC §102 (e) as being anticipated by US Patent 5,932,914 to Horiguchi. In the alternative, claims 1-20 stand rejected under 35 USC §103(a) as unpatentable over Horiguchi.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, the present invention addresses an input/output protection device of a lateral, bipolar type which quickly responds to an excess voltage pulse and/or an excess current pulse of, for example, electrostatic discharge.

In the invention, a region of a first conductor type (a fourth diffusion layer 2; all reference numerals being used herein being for exemplary purposes only and not for limiting the claims) of a semiconductor substrate, a first diffusion layer 4 of a second conduction type opposite to the first conduction type is fabricated, the layer being connected to an input/output terminal 8. A second diffusion layer 5 of the second conduction type is fabricated to be connected to electrode wiring at a fixed potential. A third diffusion layer 7 of the second conduction type is manufactured at a bottom of the second diffusion layer 5 and is connected to the second diffusion layer 5. The first diffusion layer 4 is circularly enclosed with the third diffusion layer.

When a high voltage is applied to the input/output terminal 8, a lateral, bipolar transistor including the first diffusion layer 4 as a collector, the second and third diffusion

layers 5,7, respectively, as an emitter, and the region of the first conduction type or the fourth diffusion layer 2 as a base is operated.

II. THE 35 USC §112, Second Paragraph, Rejection

Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph. Specifically, claim 1 at lines 9-10 has the unclear phrase "a second diffusion layer of the second conduction type connected to the electrode wiring kept". This claim has been amended, above, to overcome this rejection, by eliminating this phrase.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTION

A. The Horiguchi Reference (U.S. Patent No. 5,932,914)

First, Applicant respectfully asserts that this reference is disqualified as a prior art reference under 35 USC 103(c). Both the present invention and that described in the Horiguchi reference are presently commonly owned by NEC Corporation and were commonly owned at the time the present invention was made, and the present Application was filed after November 29, 1999.

Second, in complete and fundamental contrast to the claimed invention, Horiguchi provides an electrostatic breakdown protecting device which has a high electrostatic breakdown resistance, a high latch up resistance and an excellent protective ability and which

has no dead space in the vicinity of protective elements. The invention includes an I/O terminal directly connected to a protective diode comprising a p-type diffusion layer 103*a* and an n-type diffusion layer 102*b*, and an NPN protective bipolar transistor comprising n-type diffusion layers 102*b*, 102*c* and p-type well 113 and connected to an NMOSFET for protection comprising n-type diffusion layers 102*c*, 102*d* and a gate electrode 105 via an input resistor 114. These protective elements are formed on the p-type well 113 separated from a substrate for an internal circuit by an n-type buried diffusion layer 111and an n-type well 112. The internal circuit to be protected is connected to a drain 102*d* of the NMOSFET for protection.

The Examiner asserts that Horiguchi discloses

Referring to figures 1 and 2, Horiguchi discloses an input/output protection device for a semiconductor integrated circuit including a substrate 101 of the first conductive type (p type), an internal circuit, an input/output terminal, electrode wiring, and signal wiring, comprising:

a first diffusion layer 102b fabricated in a region of the first conduction type of the semiconductor substrate 101, the layer having a second conduction type (n type) opposite to the first conduction type (p type) and being connected to the input/output terminal (column 4, lines 36-37),

a second diffusion layer 102a of the second conduction type (n type) connected to the electrode wiring kept, the electrode wiring being at a predetermined potential (column 4, lines 28-31),

a third diffusion layer 112 of the second conduction type (n type) fabricated at a bottom of the second diffusion layer 102a, the third diffusion layer being connected to the second diffusion layer 102a,

the first diffusion 102b being circularly enclosed with the third diffusion layer 112 (figure1),

the first conduction type of the semiconductor including a fourth diffusion layer 103 having impurity concentration (p+) higher than that of the semiconductor substrate (p),

the third diffusion layer 112 having a depth more than that of the fourth diffusion layer 103 (figure 2),

a lateral, bipolar transistor including the fist (sic) diffusion layer as a collector, the second and third diffusion layer as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base being put to operation,

the first and the second diffusion layer being isolated from each other

by a device separating isolation layer 104 on a surface of the semiconductor, the first and second diffusion layer being manufactured with a gate electrode 105 disposed on a surface of the semiconductor substrate.

the device separating isolation layer or the gate electrode being fabricated in a circular shape (column 3, lines 20-23),

the gate electrode being connected to the signal wiring of the internal circuit of the semiconductor integrated circuit, the gate electrode being fixed to a predetermined potential, and the potential being a ground potential (column 4, lines 59-61).

3. Referring to claim 12, Horiguchi dose (sic) not show the first conduction type being a n type and the second conduction type being a p type. However, it would be obvious to one having ordinary skill in the art of the time the invention was made to form the first conduction type being a n type and the second conduction being a p type in the device of Horiguchi because the device will function the same as long as the predetermined potential is connected to a potential of a power source.

However, the device of the present invention operates quite differently from that described in Horiguchi. Specifically, in Horiguchi the second and third region form part of an n-well structure and are not used as the emitter of the transistor (column 4 lines 45 and 46). The advantage of the structure of the present invention is an improvement in switching speed.

Hence, turning to the clear language of new claim 27, there is no teaching or suggestion of "...said first diffusion layer connected to said input/output terminal serves as a collector and said second and third diffusion layers serve as an emitter for a lateral bipolar transistor."

For this reason, the claimed invention is fully patentable over Horiguchi.

Further, the other prior art of record has been reviewed, but it too even in combination with Horiguchi fails to teach or suggest the claimed invention.

IV. Formal matters and Conclusion

In view of the foregoing, Applicant submits that claims 1-27, all the claims presently

pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/5/01

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended, as follows:

1. (Amended) An input/output protection device for a semiconductor integrated circuit [including] having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, said protection device comprising:

a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite the first conduction type and being connected to the input/output terminal;

a second diffusion layer of the second conduction type [connected to the electrode wiring kept, the electrode wiring] being held at a predetermined potential; and

a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer,

the first diffusion layer being circularly enclosed with the second and third diffusion layers.